Amendments to the Specification:

Please change the title to:

METHOD FOR ~~IMPROVING~~ PROCESSING EFFICIENCY ~~OF~~ IN A PIPELINE ARCHITECTURE

Please replace Paragraph [0031] as published with the following amended paragraph:

[0031] Next, please refer to FIG. 7 to describe detailed execution steps of one of the best embodiments of the present invention. FIG. 7 is a diagram of a method for improved processing efficiency of pipeline architecture with the processor 10 as shown in FIG. 1. In the present embodiment, the first functional unit 12 is ALU and the second functional unit 14 is a MAU are assumed. Because the MAU executes a more complicated calculation task, the second function unit 14 needs an executing time period longer than an executing time period of functional unit 12. The executing time period of the first functional unit 12 is one instruction cycle, and the executing time period of the second functional unit 14 is two instruction cycles. Please note, the control unit 16 of the present embodiment generates a plurality of control signals to orderly control the first and the second functional units 12, 14 as in a first time period (as the first calculation unit in the level E1) and a second time period (as the first calculation unit in the level E2) executing the first calculation task, and in a second time period (as the second calculation unit in the level E1) and a third time period (as the second calculation unit in the level E2) executing the second calculation task. The lengths of the first, second, and third time periods are all equal to one instruction cycle, and the first, second, and third time periods are non-overlapping with one another, and the second time period is later than the first time period and the third time period is later than the second time period.

Please replace Paragraph [0041] as published with the following amended paragraph:

[0041] First, an example as mentioned above, r5=abs ((r1+r2)*r3). There are three calculation tasks needed in this calculation process. The first calculation task r0=r1+r2 is completed by utilizing the ALU, the second calculation task r4=r0*r3 is ~~completely~~ completed by utilizing the MAC, and the third calculation task r5=abs (r4) is completed by utilizing the ALU. Under an inference from a timing perspective view of above-mentioned FIGS. 4 and 5, results can come out as: utilizing the first method to execute calculation tasks, a stall of one instruction cycle occurs between the second and the third calculation tasks; utilizing the second method to execute calculation tasks, a stall of one instruction cycle occurs between the first and the second calculation tasks; and utilizing the method of the present invention to execute calculation, no stall occurs.